Fault Modeling of Sequential Circuits at Register Transfer Level

Suma M.S,K.S.Gurumurthy

Abstract— As the complexity of Very Large Scale Integration (VLSI) is growing, testing becomes tedious and tougher. As of now fault models are used to test digital circuits at the gate level or below that level. By using fault models at the lower levels, testing becomes cumbersome and will lead to delays in the design cycle. Thus there is a need to look for a new approach of testing the circuits at higher levels to speed up the design cycle. This paper proposes on Register Transfer Level (RTL) modeling for digital circuits and computing the fault coverage. The result obtained through this work establishes that the fault coverage with the RTL fault model is comparable to the gate level fault coverage.

Index Terms— fault coverage,fault list,fault models,fault simulation,RTL,stuck-at fault,test patterns.

1 INTRODUCTION

VLSI industry is growing as per Moore's law and integrated circuit designs are accordingly becoming more and more complex. As a result of this, VLSI testing has become expensive in terms of cost. Existing gate level fault simulation techniques exhibit poor performance standards when applied to such designs and are unsuitable for early testability analysis or fault simulations. Also test generation and fault simulation efforts in the post synthesis phase do not contribute to the improvement in the design. Therefore a design methodology for fault simulation at higher levels of abstraction is highly desired.

Many high-level fault models and fault simulation techniques have been proposed. No single fault model is universally acceptable since no fault model has been developed so far that comprehensively covers all classes of circuits. The RTL description is at a higher level of abstraction and may not cover all the gate level faults [2].

The fault model proposed by F.Corno, G.Cumani, M.Sonza Reorda and G.Squillero [2] adopts a particular instantiation of the observability enhanced statement coverage metric in addition to the single stuck-at bit faults on all assignments targets of the executed statements. The model implies observability enhanced statement coverage by modeling one of the possible fault classes on executed statements. This is an incomplete modeling of the various faults associated with the RTL description of the circuit.

The fault model by Barry W. Johnson is developed via abstraction of industry standard single-stuck-line (SSL) faults into the behavioral domain. A functional analysis technique was used to evaluate the effects of the SSL faults on gate-level implementation. Since the gate-level netlist changes drastically during logic synthesis, the authors in [3] concluded that modeling all possible gate-level faults at the RTL is highly inefficient.

The RTL fault model and simulation approach proposed by Mao and Gulati [4] uses the single stuck-at fault for each bit of all variables in the RTL model. The model employs both the RTL description and functional verification patterns. But their approach required one to run fault simulation twice, first in an optimistic mode and then in the pessimistic mode and to use the average of the results to reduce the difference between the RTL and the gate-level fault coverage. The experimental data shows as much as 10 % error between the actual gate-level fault coverage and the RTL fault coverage.

Another fault model proposed by Devadas and Ghosh [5] is the Observability Enhanced Statement Coverage Metric. This model requires that all statements in the RTL description are executed at least once and that their effects are propagated to at least one primary output. As this approach can be fruitfully exploited for the test pattern for fault simulation, more accurate results are needed.

The fault model proposed by Karunaratne et al. [6] does not consider stuck-at faults in the signal bit values and also not account for these faults. Also the process of locating the RTL faults and mapping them to the corresponding Gate-Level faults is to be done. It is therefore desirable to develop the fault model at a higher level of abstraction than the gate level. Fault Simulation and testing at the higher levels of abstraction have a better chance of being integrated well into the overall design process.

Jose M.Fernandes et al.[7] has proposed a new probabilistic method for controllability evaluation based on a traitorously selection of registers to form groups. This work needs further optimization by computing the probabilistic impact of the simultaneous correction of different testability problems.

The Unit II of the paper deals with the methodology, Unit III deals with the fault model and simulation Unit IV with results and finally Unit V with conclusion.

2 METHODOLOGY

In this work Verilog Hardware Description Language is used for writing the RTL models. The basic assumption is that the components are fault free and only their interconnections are affected. These map to the operators and variables in the RTL descriptions respectively. Gate level primitives can be instantiated in a model using gate instantiation as these are supported for synthesis. These primitive gates describe the hardware. Therefore synthesizing a gate primitive generates logic based on the gate behavior which eventually gets mapped to the target technology [1].Based on this the single stuck-at fault is modeled.The assumption is also that at most one fault occurs at a time in the circuit.

The proposed fault model is an improvement over the model given by Karunaratne et al.[6].Stuck-at faults in the signal bit values was not considered and accounted. Also the process of locating the RTL faults and mapping them to the corresponding Gate-Level faults was not implemented.

The analysis flow for the modeling approach is of two ways as shown in Fig. 1. One way targets on the gate-level fault coverage while the other is on the RTL fault coverage. In the RTL path, the RTL design description is obtained based on the specification. Since the fault model is at the RTL, the fault is induced at the input and at the output. This is done by using a buffer for each bit in all of the variables in the RTL code. These buffers are inserted in the fault free circuit and should not disturb the functionality of the code. As a result, a modified faulty RTL circuit is obtained. To enable fault simulation the process of generating faulty circuits by inducing faults into the fault-free circuit is done. For each of the faults a new circuit is created.

Testbench is developed and the simulation is first run on a good circuit and then on each of the faulty circuits using any simulator. The outputs obtained in each case of the faulty circuits are compared with the output of the good circuit to determine which faults are detected. That is the new faulty circuit and the fault free circuit is simulated and the outputs so obtained are compared. The fault list is tabulated. The ratio of the numbers of RTL faults detected to the total number of RTL faults gives the RTL fault coverage. For each RTL design descriptions gate level implementations are obtained for 65 nanometer target technology using logic synthesis tool and fault cover
age obtained by Tetramax tool. The fault list of both the RTL as well as Gate-Level faults is compared. The effectiveness of our fault model is determined by comparing RTL fault coverage with the fault coverage obtained at the gate level.

3 RTL FAULT MODEL AND SIMULATION

It is difficult to generate test for real defects due to the diversity of VLSI defects. For generating and evaluating a set of test patterns,fault models are needed. Widely a good fault model should almost give a true nature of the behavior of defects and it should also computationally work well in terms of fault simulation and test pattern generation. It is necessary to propose a fault model, that is a fault model for how faults occur and their impact on circuits and to do with the business of good and bad parts, many fault models have been proposed [4], but unfortunately, no single fault model accurately reflects the behaviour of all possible defects that can occur. As a result, a combination of different fault models at many instances are used in the generation and evaluation of test vectors and testing approaches developed for VLSI devices [2]. Developing a test for faults at higher level of abstraction and then determining the percentage of faults at the lower levels being covered is a good strategy. Fault models at higher levels result in significant savings in test cost and test time required for deriving tests.

The most common model used for logical fault is the single stuck-at fault (SSF). In this a fault in a logic gate gives a favourable outcome in one of its inputs or the output being fixed to either a logic 0(stuck-at-0) or a logic 1(stuck-at-1).

For our approach up-down counter is taken as an example.

```
module count_up_down #(parameter width
= 3)(
  output    reg [width:0] count,
 output     scanout,
 input      [width:0] data,
 input          load, Up, clear, clock
);
     always@(posedge clock, negedge
clear)
if(!clear)  count <=
{(width+1){1'b0}};
     else  if (load)   count <= data;
else  if (Up)     count <= count +
1'b1;
else              count <= count -
1'b1;
endmodule
```

The above RTL design description is a fault free module. Faulty module is created such that the functionality will remain same as the fault free module .This is done by inserting the buffer for each of the ports. The faulty module appears as shown below.

```
module count_up_down #(parameter width
= 3)(
 output      [width:0] count,
 input       [width:0] data,
 input           load, Up, clear,
clock );

reg [width:0] count_fault;
wire [width:0] data_fault;
wire
load_fault,clear_fault,clock_fault,Up_
fault;

buf L1(load_fault,load);
buf U1(Up_fault,Up);
buf C1(clear_fault,clear);
buf C2(clock_fault,clock);
buf D0(data_fault[0],data[0]);
buf D1(data_fault[1],data[1]);
buf D2(data_fault[2],data[2]);
buf D3(data_fault[3],data[3]);
buf CT0(count[0],count_fault[0]);
buf CT1(count[1],count_fault[1]);
buf CT2(count[2],count_fault[2]);
buf CT3(count[3],count_fault[3]);


      always@(posedge clock_fault,
negedge clear_fault)

                  if(!clear_fault)
      count_fault <=
{(width+1){1'b0}};
            else  if (load_fault)
      count_fault <= data_fault;
            else  if (Up_fault)
      count_fault <= count_fault +
1'b1;
            else
count_fault <= count_fault - 1'b1;

endmodule
```

To these faulty and fault free modules fault simulation is performed with the reduced number of test patterns for each of the faults.The simulated waveform for the output stuck–at 0101 is as shown in Fig. 2

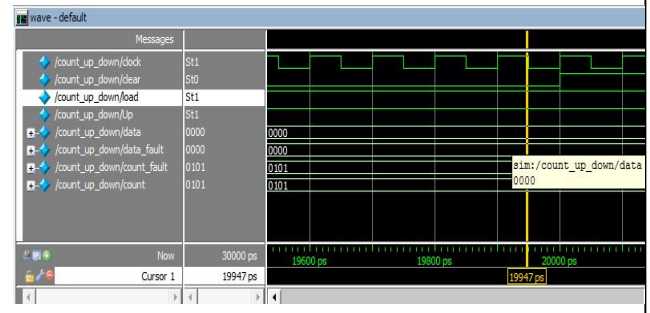

Fig.2 Waveform for the output stuck-at 0101

4 Results

At the writing of this paper, we have tested our approach on combinational logic circuits and sequential circuits. The results obtained by applying our approach to the RTL design descriptions and their corresponding Gate-level descriptions have been tabulated in table 1. At the gate-level, the gate-level netlist is created for each of the circuit used. Fault coverage is obtained for the scan inserted gate-level netlists. From the results it can be observed that the RTL Fault Coverage obtained by the proposed fault modeling methodology has a close match to the Gate-level Fault Coverage for the tested digital circuits.

TABLE 1
RTL VERSUS GATE-LEVEL FAULT COVERAGE

Name of the circuit	RTL Fault Coverage	Gate-Level Fault Coverage
JK flip-flop	100%	100%
D flip-flop	100%	100%
Updown counter	100%	100%
Johnson counter	100%	100%

5 Conclusion

With the progress of semiconductor technology testing of VLSI circuits becomes more and more difficult and at the same time cost is also increasing. Therefore it is important to achieve high fault efficiency with low cost. With this approach RTL designer can have an estimation of the achieved fault coverage before doing synthesis and also it is possible for the designer to locate faults at a higher level of abstraction. At present our approach is applied to combinational logic circuits and few sequential logic circuits. In future we would like to extend the approach to complex sequential circuits such that there is a close match to the gate level fault coverage and hence reducing the impact on time to market.

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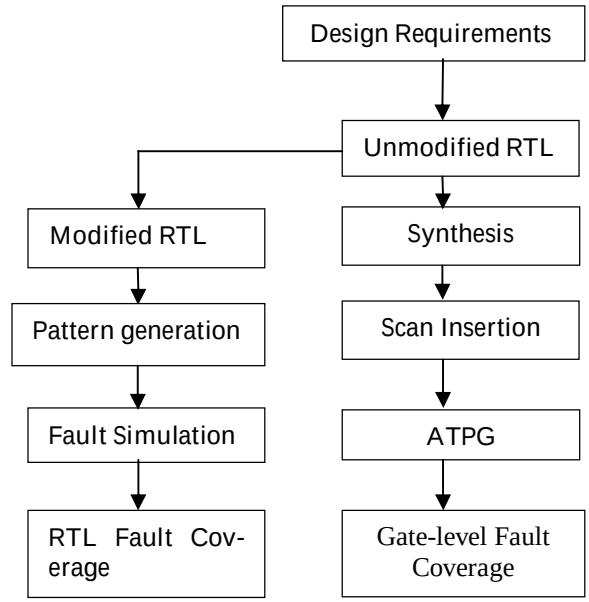

Fig. 1. Design flow with the proposed method